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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/573,970	03/30/2006	Tatsuo Hiramatsu	070456-0105	1749

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EXAMINER	
GIROUX, GEORGE	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
12/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,970	HIRAMATSU ET AL.	
	Examiner	Art Unit	
	GEORGE D. GIROUX	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12 May 2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 11 August 2009, in response to the Office Action mailed 11 May 2009. The applicant's remarks and any amendments to the claims or specification were considered, with the results that follow.

2. Claims 1-48 have been cancelled, while new claim 49 has been added. Claim 49 now stands pending in this application.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 49 is objected to because of the following informalities: it is not entirely clear what is meant by "...." in the claim language. It appears, to the examiner, that the applicant intended that data A and B is being divided into a number, L, of units labeled A1, A2 through AL and B1, B2 through BL, respectively. Appropriate correction is required.

5. Claim 49 is further objected to because of the following informalities: it is not entirely clear, from the claim language, whether the final limitation (setting A2 to the first stage, B1 to the Nth stage and the output of A1 to the first stage) is done at the same "one time point" as setting A1 to the Nth stages (which appears to contradict the specification, as A1 and B1 would both be set to the same stage), or whether "at a next time point" was inadvertently left off of the end of the claim. It appears, to the examiner, that the applicant intended the latter. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schmit (Incremental Reconfiguration for Pipelined Applications, April 1997, pages 47-55) in view of Kelsey (US 2002/0002667).

As per claim 49, Schmit teaches a reconfigurable circuit consisting of N stages, where N>1 **[a striped FPGA consisting of a number (11 in the figure) of stripes (page 48, figure 1)]**, each of the stages having a plurality of arithmetic units as **[each stripe includes a number of cells (page 54, figure 11), where each cell can function as several things, including an ALU (page 54, section 5.0)]**, an internal state holding circuit located between the stages as **[registers are connected to the**

outputs of the cells in each stripe (page 54, section 5.0)], and a control portion **[control unit and configuration cache (page 53, figure 10)]** controlling setting data so that setting data A and B are successively supplied to the reconfigurable circuit to configure an intended circuit as **[the control mechanism loads the application, which has been broken down into a set of "stripes", onto the striped FGPA successively in a pipelined fashion (page 53, section 4.0 and figures 9 & 10)]**, the data A and B being divided into units A1, A2, ... and B1, B2, ..., etc., as **[the control mechanism loads the application, which has been broken down into a set of "stripes", onto the striped FGPA successively in a pipelined fashion (page 53, section 4.0 and figures 9b & 10) where figure 9b shows the divided setting data (f_1, f_2, etc.)]**.

While Schmit teaches successively setting the portions of the application circuit to stripes in the FPGA and passing outputs between stages across time points (page 53, figure 9b), Schmit does not teach that A and B are separate configurations divided respectively, and wherein, when the unit A1 is set to an Mth stage at one time point (where N>M>1), the control portion sets the unit A2 to an (M+1)th stage, sets the unit B1 to the Mth stage and sets output data of the unit A1 to the (M+1)th stage at a next time point, and when the unit A1 is set to an Nth stage at one time point, the control portion sets the unit A2 to the first stage, sets the unit B1 to the Nth stage and sets the output data of the unit A1 to the first stage.

Kelsey teaches switching between threads/contexts every cycle as **[the system switches context every cycle within a small, finite (or zero) time between contexts**

(paragraphs 0049-0052)] and passing the outputs of one stage executing a context to another stage executing that same context (though a different instruction/function associated with the context) as **[a context number is also passed with each instruction down the pipeline determine which context registers are used to load the program counter, load register values from or to save register values to, etc. (paragraph 0052)]**.

Schmit and Kelsey are analogous art, as they are within the same field of endeavor, namely pipelining execution.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to switch contexts each pipeline cycle and passing data between stages executing the same context at different time points, as taught by Kelsey, in the pipelined stripe FGPA reconfiguring and processing taught by Schmit, such that the circuit configuration contexts (i.e., configurations for different circuits) are switched between time points in the striped FGPA. In figure 9b of Schmit, this would roughly equate to replacing f_1 with fA_1, f_2 with fB_1, f_3 with fC_1, f_4 with fA_2, etc. and passing the output data of fA_1 as inputs to fA_2.

This would create a striped FGPA in which, when the unit A1 is set to an Mth stage at one time point (where N>M>1), the control portion sets the unit A2 to an (M+1)th stage, sets the unit B1 to the Mth stage and sets output data of the unit A1 to the (M+1)th stage at a next time point, and when the unit A1 is set to an Nth stage at one time point, the control portion sets the unit A2 to the first stage, sets the unit B1 to the Nth stage and sets the output data of the unit A1 to the first stage.

The motivation for doing so would be to increase throughput, and reduce the total execution time for multiple circuit execution, by overlapping the execution on several circuit configurations, as well as **[switching contexts every cycle eliminates the penalty due to the loss of work required by a pipeline flush in a single context, as the pipeline has work from the other threads to do in the meantime (paragraph 0050) and eliminates much of the overhead otherwise required for switching between contexts (paragraphs 0012-0014)]**, as provided by Kelsey, which would be applicable to the pipelined structure of execution taught by Schmit using circuit configuration contexts.

Response to Arguments

8. Applicant's arguments, see pages 3-4 of the remarks, filed 11 August 2009, with respect to the rejection(s) of claim(s) 34 and 37-42 under 35 U.S.C. 103(a) have been fully considered and are persuasive (i.e., these claims have all been cancelled, and the cited art of record does not teach or suggest all of the new claimed limitations). Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Schmit (Incremental Reconfiguration for Pipelined Applications, April 1997, pages 47-55) and Kelsey (US 2002/0002667).

Schmit teaches a "striped FPGA" in which segments of the FGPA are sequentially and successively reconfigured each cycle in a pipelined fashion, while Kelsey teaches a pipeline which switches contexts every cycle and passes the outputs

of one stage executing a context to another stage executing that same context (though a different instruction/function associated with the context)

Conclusion

9. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 1-48 are cancelled; claim 49 is rejected.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Trimberger et al. (A Time-Multiplexed FPGA, 1997, pages 22-28) -- discloses a FPGA system, similar to that disclosed by Schmit, which uses micro registers to pass data between stages.

b. Serrano (US 2006/0126454) -- discloses processing for a demodulator, including a loop filter and positive/negative peak determination.

c. Naoi (US 2003/0200237) -- discloses a pipeline of programmable arithmetic logic units that can be controlled individually or operated together and work in a cascade fashion.

d. Vorbach (US 2006/0248317) - teaches a reconfigurable circuit which can be divided dynamically to perform given operations.

e. Vorbach (US 7,003,660) -- discloses pipelining configurable processing units.

f. Pickett (US 4,942,319) -- discloses multiple programmable pages configured into a programmable array, including moving signals between.

12. The examiner requests, in response to this Office action, that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

13. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEORGE D. GIROUX whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183

/George D Giroux/
Examiner, Art Unit 2183